REMARKS

The Examiner is thanked for carefully reviewing the present application. The present amendment is in response to the first Office Action mailed on May 5, 2005 regarding claims 1-28.

Favorable reconsideration is requested in view of the above amendments and the following remarks.

Claims 13 and 28 are cancelled and the limitations thereof are respectively added to claims 1 and 25. Claims 29-30 are added to include the limitations of claims 14 and 20. Thus, claims 1-12, 14-27 and 29-30 are now pending in the application. The amended claims and the new claims contain no new matter nor raises new issues.

Claim Objections

Claims 6 and 7 are objected to because of the following informalities: Claim 6, line 2 and claim 7, line 4 "...the BIST circuit..." lacks antecedent basis.

In response thereto, claims 6 and 7 are amended in accordance with the suggestion made by Examiner to change "...the BIST circuit..." to "...a BIST circuit...".

After amendment, claims 6 and 7 are now believed to be in form for allowance. Accordingly, Applicant respectfully requests that the claim objections be withdrawn.

Allowable Subject Matter

Applicant notes with appreciation the Examiner's indication in Allowable Subject Matter that claims 7, 13, 20 and 28 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Therefore, claims 13 and 20 are cancelled and the limitations thereof are respectively added to claims 1 and 25; and claims 29-30 are added to include the limitations of claims 20 and its base claim 14. Accordingly, claims 1, 25 and 29 are now believed to be in form for allowance.

Claim Rejections under 35 U.S.C. §102(e)

Claims 1-6, 8-12, 14-19 and 21-27 are rejected under 35 U.S.C. §102(e), as being anticipated by Ober et al. (US 6,708,273). These rejections are respectfully traversed.

As explicitly recited in claims 14 and 15, the accelerated test system of the claimed invention comprises an a utomated test equipment, a one-way-hash module and a comparator, wherein the one-way-hash module can be implemented in an integrated circuit to be tested (see claims 19-20) or in the automated test equipment (see claims 21-24). The automated test equipment sends test vector data to the integrated circuit, and the integrated circuit produces response data in response to the test vector data, and the one-way-hash module receives the response data and generates a test message digest, and then the automated test equipment receives the test message digest to be verified against a standard digest.

In contrast, such as shown in Fig. 1 and the related specification, Ober's apparatus is directed to a secure communication platform on an integrated circuit, which is not an accelerated test system for testing an integrated circuit as explicitly recited in the claimed invention. Ober does not teach or suggest any components disclosed in claims 14 and 15 of the claimed invention, and Ober's hash circuit coupled with the encryption circuit for performing hash-then-encrypt and hash-then-decrypt operations (see column 6 lines 4-17).

The Federal Circuit reiterated that "a rejection for anticipation under section 102 requires that each and every limitation of the claimed invention be disclosed in a single prior art reference." In re Paulsen, 31 USPQ 2d 1671 (Fed. Cir. 1994).

Accordingly, since Ober's apparatus is not the accelerated test system for testing the integrated circuit as taught in claim 14, claim 14 of the claimed invention cannot be anticipated by Ober.

Likewise, by virtue of their dependence on patentable claims 14, claims 15-24 are also patentable over Ober. Accordingly, Applicant respectfully requests that the section 102(e) rejections be withdrawn.

CONCLUSION

With regard to other prior arts made of record in the Office Action, Walmsley et al. (US 6,374,354), Kaplan et al. (US 6,704,871), Silverbrook et al. (US 6,757,832), Walmsley (US 6,816,963), Sheu (US 6,507,800) and Williams et al. (US 2004/01333831); and non-patent references of Ferrari, Post, Brosa and Kitsos all do not disclose or teach the accelerated test system for testing the integrated circuit disclosed in claimed invention.

In light of the above remarks, all objections and rejections having been addressed, it is respectfully submitted that the present application is in a condition for allowance and a Notice to that effect is earnestly solicited. If there are any remaining issues to be resolved, the applicant requests that the Examiner contact the undersigned attorney for a telephone interview.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 07-1337 and please credit any excess fees to such deposit account.

Respectfully submitted,

LOWE HAUPTMAN & BERNER, LLP

Benjamin J. Hauptman
Registration No. 29,310

Customer Number: 22429
1700 Diagonal Road, Suite 300
Alexandria, Virginia 22314
(703) 684-1111
(703) 518-5499 Facsimile
Date: August 2, 2005
BJH/jk